USE OF MULTIPLE CIRCUIT ELEMENTS FOR BACK SIDE CONNECTION TO A FLAT PANEL DISPLAY

BACKGROUND OF THE INVENTION

The present disclosure relates to the field of interconnections to flat panel displays, and more specifically to a display panel structured for attachment of multiple circuits using a two-dimensional array of contacts.

A conventional display panel includes a plurality of display cells operative to render an image. Provided for the display cells are display contacts configured to receive a driver circuit to drive the display cells. The driver circuits are generally mounted on the edge of the display panel. Presently, interconnections between a flat panel display and other electronic components, such as driver circuits, are made in several ways.

Multiple contacts on a panel edge can be attached to an interconnection element, such as a flex circuit. These elements then provide interconnection to separate circuit boards. Alternatively, an integrated circuit can be bonded directly to an edge of the flat panel display. Lastly, thin film transistors can be fabricated directly on the display glass and used to provide driver and function controls.

These approaches require additional area around the display edge. Because a plurality of drivers are located in the peripheral region of the display panel in an edge connection arrangement, fabrication and processing steps are costlier than conventional processes. Panels using thin film transistors also have greater fabrication costs compared to conventional display panels.

The above-described edge connection scheme can further contribute to increased line resistance or capacitance, which may adversely affect the performance of the display. Additionally, the edge connection approach may require an undesirably high voltage level to drive the pixels. In some cases, the edge connections can require a significant mounting area in the peripheral region of the display, thereby limiting the area available for the display itself and increasing cost, manufacturing difficulty, and panel durability.

One solution to the above problems has been to form larger flat panel displays from smaller display units by tiling the smaller display units. Individual display units or tiles are usually arranged in an array and attached to each other

along the edges of the display tiles, thereby forming a single tiled flat panel display of larger size.

These approaches are limited by the use of a single circuit board back panel to effect interconnection to the display front panel. As the size of the display increases or the pitch of the array contacts decreases, increasing demand is placed on the flatness requirements for the panels.

A further disadvantage of tiling is that routing of contacts between the display cells and the driver circuits are constrained by the edge connections. Moreover, seams between the adjacent display tiles must be concealed so that the final assembled flat-panel display can be viewed as a seamless single display unit. One approach to solve this problem is employment of a black matrix on an optical integration plate that aligns with the individual pixels on the display tiles. While this approach is successful, it increases production costs and imposes limitations on display size and shape.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a front view diagram of a prior art display panel with a plurality of contacts distributed around the edge of the panel.

FIG. 2 is a front view diagram of a panel constructed according to the present disclosure.

FIG. 3 is an enlarged front view diagram of a portion of the panel of FIG. 2.

FIG. 4 is a partial cross-sectional diagram of the panel of FIG. 2.

FIG. 5 is a perspective diagram of the panel of FIG. 2 having a driver circuit board attached thereto.

FIG. 6 is a view of the panel similar to FIG. 5 with multiple driver circuit boards mounted thereon.

FIG. 7 is a view of the panel similar to FIG. 5 with a plurality of driver circuit boards mounted in the central region of the panel.

DETAILED DESCRIPTION OF EMBODIMENTS

FIG. 1 shows a prior art panel 10 having contacts 12 for driver circuits. The contacts 12 are conventionally distributed about the edge of the panel.

An exemplary embodiment of a display panel as disclosed herein is illustrated in FIGS. 2-4. The panel 20 has a front side 22 and a back side 24 and further includes a peripheral region 26 and a central region 28.

A pattern of contacts 30 is distributed on the back side 24 of the panel 20. The pattern is disposed in the central region 28 as well as the peripheral region 26. The pattern of contacts constitutes a matrix of interconnection points. The contacts can be bond pads or other structure suitable for forming an interconnect between the panel and a component.

The pattern of contacts is selectively placed to connect a component, (e.g., a circuit board, an integrated circuit, or other passive or active component) to the display contacts 22 in the panel. For illustrative purposes, the pattern is shown as a regular two-dimensional array of contacts. It should be readily apparent that the pattern of contacts need not be regularly and uniformly arrayed, but can be disposed on the back side of the panel in numerous alternative arrangements. Such arrangements are motivated by considerations, e.g., driver circuit placement and display device dimensions.

A panel as disclosed herein is shown in partial cross-section in FIG. 4. The display panel comprises a panel 40 having a plurality of conventional display cells 42 disposed on the front side 22 or within the panel. The display cells have pixels therein which are illuminated so as to electrically display an image. The display cells are controlled by a driver circuit coupled thereto via display cell contacts 44. Such display cells are known in the art.

On the back side 24 of the panel is an insulating layer 46 and an electrically conductive circuit layer 54. The circuit layer in this embodiment comprises traces routed from the display cell contacts 44 to the pattern of contacts for the driver circuit 30.

The pattern of contacts 30 of the circuit layer 54 is coupled to display contacts 44 for display cells in the panel. Display contacts 44 are thereby coupled the display cells to an electrically conductive circuit layer 54. The original front panel contacts can be used as the attachment points for the multiple boards. Alternatively, the above described circuit layer can be utilized as the set of driver circuit connects. While this description implies the use of a single insulating layer 54, contacts 44 and circuit pattern 54, this concept can obviously be extended to multiple layers,

providing for increased complexity in the front screen interconnection circuit, as needed by system or cost considerations.

In a preferred alternative embodiment, electrically conductive traces are routed through a second electrically conductive circuit layer 50, permitting greater freedom in placement of the driver circuit interconnects 30. In this embodiment, a second ceramic or insulating layer 52 is provided, and the first electrically conductive circuit layer 54 (or bond pad layer) provides the pattern of contacts for the driver circuit attachment.

In another embodiment, a panel constructed as in FIGS. 2-4 further can accept a plurality of components on the back side of the panel and in the central region. For example, a panel 20 can have a circuit board 60 attached to the back side 24 in both the central region 28 and the peripheral region 26 (FIG. 5). Multiple circuit boards, with components already attached, can be attached to the back side of the display panel, either directly to the two-dimensional array of contacts on the panel or to the interconnection circuit described above.

FIG. 6 shows a panel constructed according to the present disclosure and having attached to the back side 24 of the panel 20 three circuit boards 60A, 60B and 60C. Placement of the plurality of components is not limited positionally with respect to the panel. For example, a subset of the plurality of components can be connected in the central region and a second subset connected in the peripheral region. The circuit boards can be connected to span both the peripheral and central regions (FIG. 6).

Alternatively, circuit boards smaller than the front panel can be connected to the panel. FIG. 7 shows a panel 20 having attached four circuit boards 60A-60D. The panel is configured so that the circuit boards are mounted in the central region. This configuration permits connection to the display panel of multiple driver circuits or components via contacts fabricated on the back of the display, without the requirement that components be localized to the edge of the panel. Components, such as circuit boards or integrated circuits, can be attached directly to the panel back at virtually any point thereon.

With such an attachment, the edge of the panel can remain free of electrically conductive contacts. The configuration further minimizes the panel dimension requirements. As well, panel planarity restrictions are avoided and testability is increased.

A further advantage of the present panel is that traces coupling the display cell contacts to the bond pads need not be routed to the panel edge. Therefore, trace runs are generally shorter, and the present panel allows greater freedom in X- and Y-axis routing of traces.

Prior art display panels typically have multiple circuits driving multiple emissive displays. The multiple emissive are tiled into one display panel, typically using an interface plate. The present panel can use multiple circuits to drive a single monolithic display. The electronics can be tiled, but the emissive display tiling requirement is removed.

Because the display is not tiled, no interface plate is required. Benefits of the obviation of the interface plate include better optical quality of the display and greater efficiency. The panel configured as disclosed herein is also simpler and cheaper to manufacture.

Mechanical advantages are also realized, in that thermal stresses can be better distributed. The panel and interface plate usually have varying coefficients of thermal expansion (CTE), and expansion and contraction can cause deformation of the panel. The present panel eliminates the need for the plate and spreads remaining thermal stress by localizing it to the circuit boards attached to the display.

This scheme enables a direct attachment approach, such as the chip-on-glass approach employed for LCD manufacturing, while giving the additional advantage of decoupling the interconnect layout requirements of the components from that of the display. These benefits in turn permit concurrent engineering of components and displays with less risk. In addition, this scheme can be exploited to provide additional benefits, such as increased reliability and manufacturing yield through contact redundancy.

In this approach, there may be a need to attach components to the interconnect structure subsequent to fabrication of the display. Temperature limitations associated with the display materials may exist, and such limitations may be inconsistent with the solder temperatures required for the component attachment processes.

In such a case, the components can be pre-attached to smaller circuit boards, which boards can then be attached to the display front panel using an attachment process compatible with the display materials. These smaller boards relax the

flatness tolerance requirements placed on an equivalent-sized large board. Smaller boards also provide flexibility in design, purchasing and testing.

While the illustrated embodiment has shown circuit boards attached to the panel, other components can be similarly mounted directly to the interconnection circuit described above. Such components can be active (e.g., integrated circuits) and passive (e.g., resistors, capacitors, connectors) components.

The multiple board approach has the added advantage over direct attachment of integrated circuits of permitting the circuit boards to be pre-tested and, if needed, burned-in prior to attachment to the display panel.

A circuit can be built up directly on the back side of the panel, utilizing the central region in addition to the peripheral region or edge of the panel. The circuit then can be used to connect components. Interconnection circuits are preferably fabricated by using subtractive printed circuit board processes.

The display panel includes an array of display contacts, a layer of conductive circuit lines, and the pattern of contacts.

The circuit board fabrication process introduces a conformal back panel, eliminating the flatness requirement. This approach has an added advantage, in that the circuit board can be fabricated on a large glass panel that can be later excised into separate displays.

The process for fabricating a display panel as shown in FIG. 4 entails providing a panel having a plurality of display cells distributed within it.

A display contact layer is formed on one side of the panel. The display contact layer is a two-dimensional array of display contacts coupled to the plurality of display cells. A first insulating layer is deposited onto the display contact layer, with contact vias opened in the insulating layer to provide interconnection between layers. A first electrically conductive circuit layer is formed on the first insulating layer. In this embodiment, the first electrically conductive circuit layer comprises the pattern of interconnects or bond pads to which a component can be attached. The bond pads are structured to have connected thereto one or more components.

Alternatively, the first conductive layer may comprise a plurality of traces routed to the array of display contacts. A second insulating layer is then deposited, and a bond pad layer is formed thereon. Again, vias in the second insulating layer are need to provide interlayer connection. The bond pad layer is coupled to the

circuit layer, and is substantially disposed within the central region of the first side of the panel.

The panel as described herein can be incorporated into a variety of devices desiring a flat panel display. The device generally will provide an image generator (e.g., a processor) and a display interface coupling the image generator to the display panel. Such devices include, for example, cellular telephones, palm-top computing devices such as computers and digital assistance devices, and gaming devices.

In prior art panels, each display cell generally does not have its own contact. In a standard display, for example, the number of contacts is equal to the number of columns plus the number of rows. By contrast, the number of contacts in the present panel exceeds that sum, although there are not necessarily as many contacts as there are cells.

A person skilled in the art will be able to make and use the display panel in view of the description present in this document, which is to be taken as a whole. The specific embodiments herein disclosed and illustrated are not to be considered in a limiting sense. Indeed, it should be readily apparent to those skilled in the art in view of the present description that the panel can be modified in numerous ways. The inventor regards the subject matter of the invention to include all combinations and sub-combinations of the various elements, features, functions and/or properties disclosed herein.